**Amendments to the Claims:**

**Listing of Claims:**

Claim 1 (currently amended) A method for implementing circuit layouts in a chip, comprising:

forming a plurality of sub-circuit cells with the same layout in different positions of the chip, where each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal, each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas;

when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells, wherein each layout in the connection layer corresponding to each sub-circuit cell creates a connection between some of the sub-circuit blocks within each corresponding sub-circuit cell by selectively connecting the sub-circuit blocks within each corresponding sub-circuit cell ~~, and short-circuits the rest of the sub-circuit blocks within each sub-circuit cell not connected together to DC bias voltages of the chip,~~ so that the sub-circuit cells in different positions implement different circuit functions.

Claim 2 (original) The method of claim 1, wherein the connection layer is a metal layer.

Claim 3 (original) The method of claim 1, the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer.

Claim 4 (cancelled)

Claim 5 (original) The method of claim 1, wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuits with different I/O functions.

Claim 6 (original) The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with a Schmidt trigger function.

Claim 7 (original) The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with different slew rates.

Claim 8 (original) The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with different driving currents.

Claim 9 (currently amended) A chip, comprising:

a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout, each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal [[;]] and each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas;

at least a connection layer comprising different layouts corresponding to the different positions of the layout layers, wherein each layout of the connection layer creates a connection between some of the sub-circuit blocks within each corresponding sub-circuit cell, ~~and short-circuits the rest of the sub-circuit blocks within each sub-circuit cell not connected together to DC bias voltages of the chip,~~ so that the sub-circuit cells in different positions implement different circuit functions.

Claim 10 (original) The chip of claim 9, wherein the connection layer is a metal layer.

Claim 11 (cancelled)

Claim 12(original) The chip of claim 9, wherein the connection layer implements input/output (I/O) circuits with different I/O functions by the sub-circuit cells in different positions.

Claim 13 (original) The chip of claim 12, wherein the connection layer implements I/O circuits with a Schmidt trigger function with the sub-circuit cells in different positions.

Claim 14 (original) The chip of claim 12, wherein the connection layer implements I/O circuits with different slew rates with the sub-circuit cells in different positions.

Claim 15 (original) The chip of claim 12, wherein the connection layer implements I/O circuits with different driving currents with the sub-circuit cells in different positions.